Mercury 2 FPGA Module
Reference Manual

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OVERVIEW

Mercury 2 is an ultra-compact 3" x 1" Xilinx Artix-7 FPGA development board. The convenient 64-pin DIP form-factor makes it easy to add an FPGA to a breadboard, protoboard, or to your own custom PCB design. The *Mercury 2* module provides a complete FPGA solution, encapsulating all the required power, configuration, and I/O circuitry, leaving you to focus on your project.

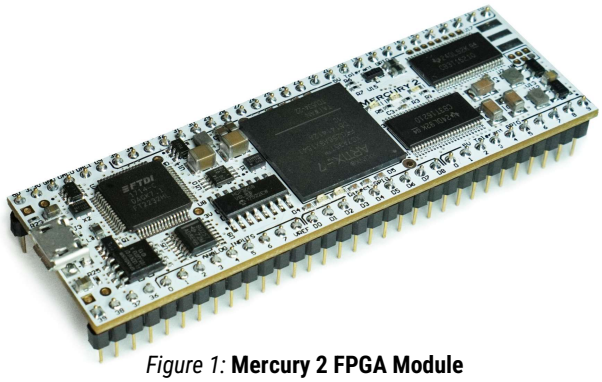

Figure 1: **Mercury 2 FPGA Module**

Unlike most FPGA development boards, *Mercury 2* is equipped with 5V tolerance on 40 digital I/O pins, so FPGA logic can be safely and easily interfaced with 5V logic level devices. The *Mercury 2* board also supports a wide range of analog I/O, including an 8-channel SPI ADC with external VREF up to 5V, a 2-channel SPI DAC, and the 1-MSPS Xilinx XADC. An external 4Mbit SRAM provides a high-speed buffer for data acquisition and signal processing.

Mercury 2 has a 32 Mb SPI flash to hold the FPGA bitstream and user data. The board has a micro USB port for easy programming and user data transfer. The board is also equipped with a 10/100 Ethernet PHY for network connectivity.

The complete schematics for *Mercury 2* are available on our website, along with open-source USB programmer apps for Windows and Linux, and several example projects, and reference designs.

SPECIFICATIONS

- Xilinx Artix-7 FPGA (XC7A35T-1FTG256C)
  - 33,280 logic cells
  - 1,800 Kbits internal block RAM
  - 90 DSP slices (DSP48E1 48-bit ALUs)
  - 5 clock management tiles (CMT)
- FTDI FT2232H dual-channel 480Mbps USB 2.0 interface with Micro-USB port
  - Channel A: FPGA configuration and debug
  - Channel B: user-configurable interface for high-speed data transfer
- 32 Mbit SPI flash (up to 16.7 Mbit used for FPGA bitstream, remainder for user data)
- 4 Mbit SRAM (512 K x 8 bit) with fast, asynchronous 10 ns interface
- 50MHz MEMS oscillator (±50 ppm)
- Digital input/output
  - 40x 5V tolerant digital I/O pins (SN74CB3T)
  - 10x FPGA-direct I/O pins
  - 3x user LEDs
- Analog input/output
  - 8-channel, 200 KSPS 10-bit ADC (MCP3008)
  - 2-channel, 220 KSPS 10-bit DAC (MCP4812)
  - 1 MSPS 12-bit Xilinx XADC module (1x direct input and 3x AUX inputs)
- Network communications
  - 10/100 Ethernet PHY (Microchip LAN8720A) for use with Ethernet jack breakout board
  - Expansion header (1x8 pin, 0.05") intended for use with the ESP-11 Wi-Fi module

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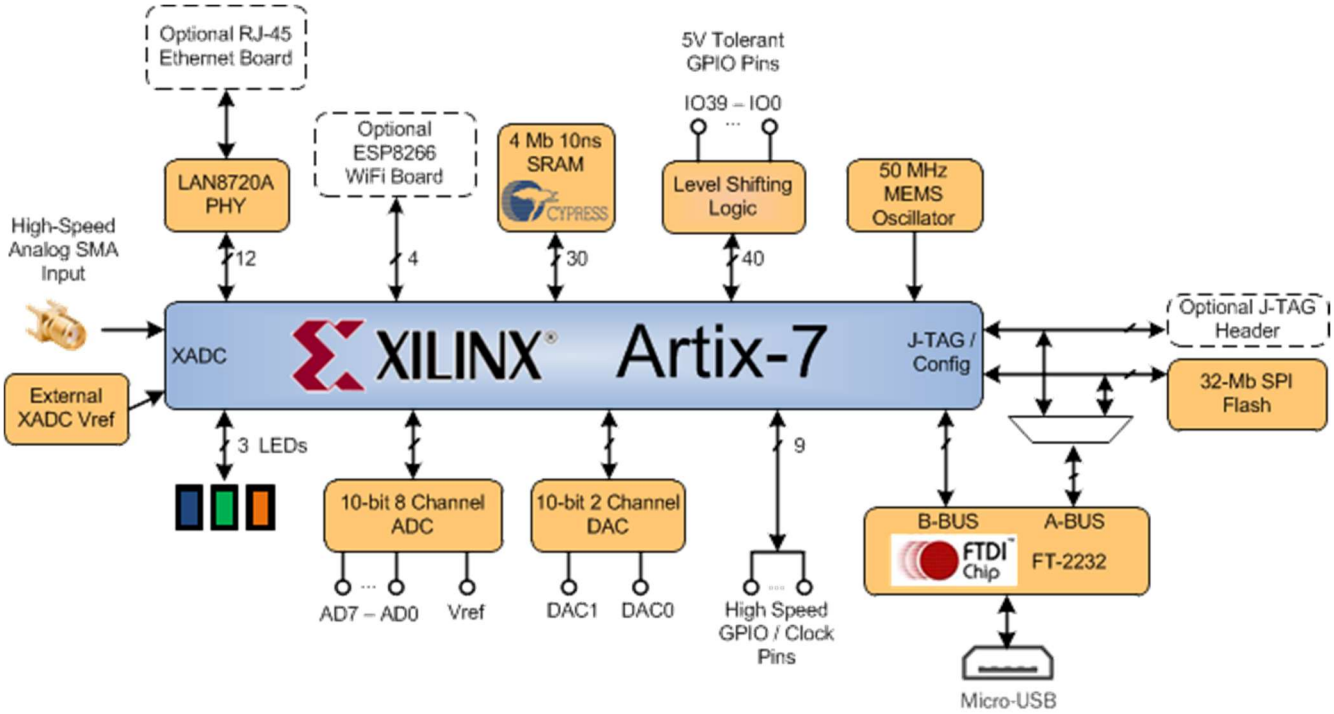

Figure 2: **Simplified Block Diagram**

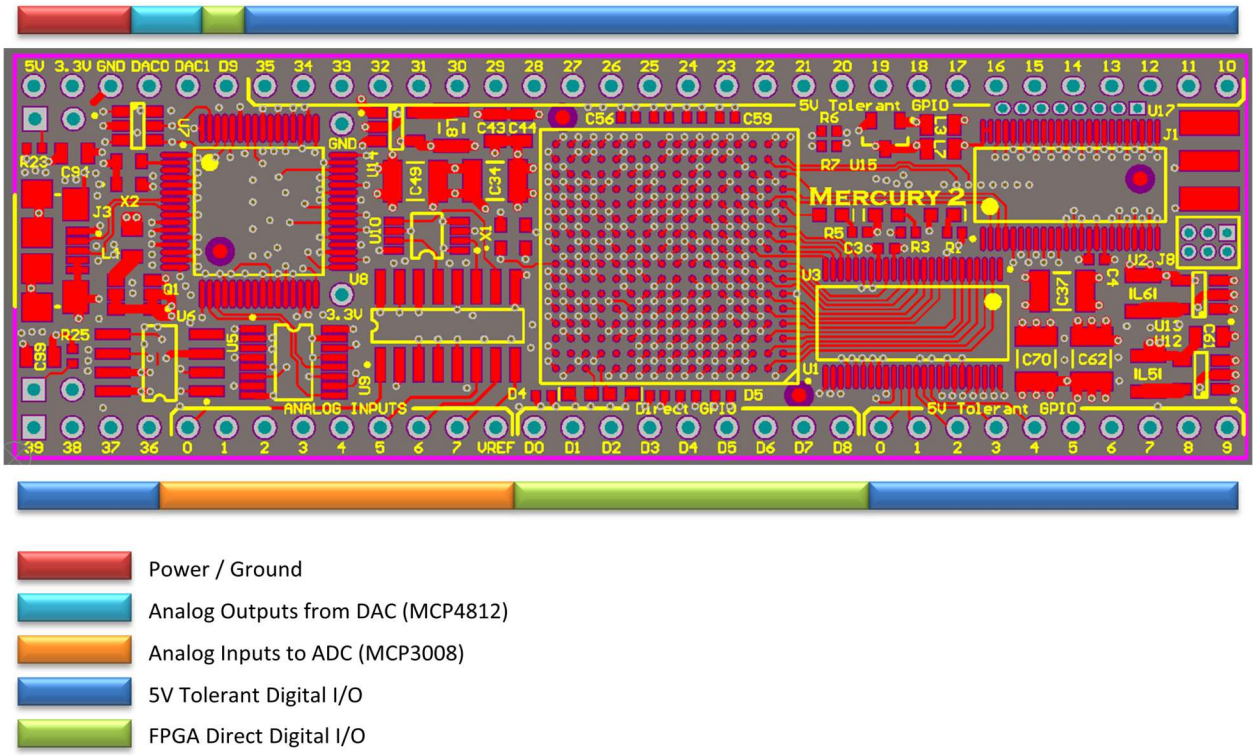

Figure 3: **DIP Pin Distribution**

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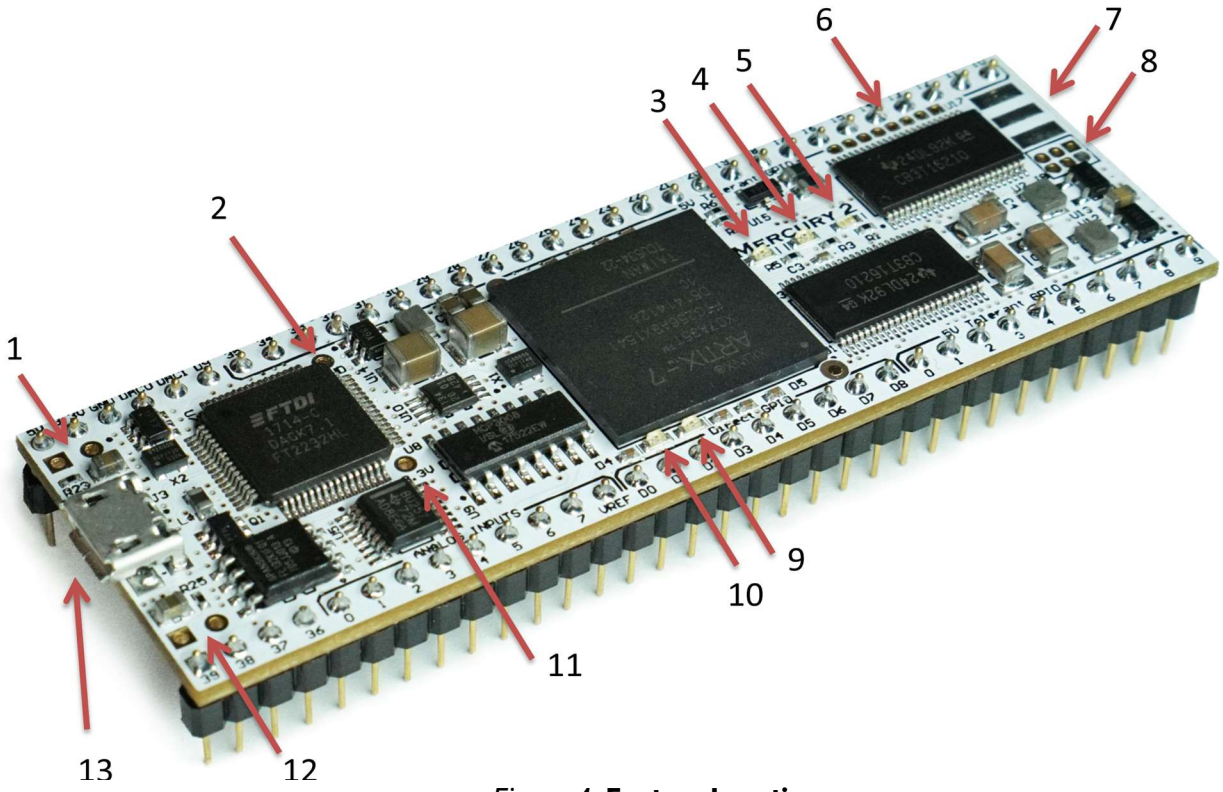

Figure 4: **Feature Locations**

CALLOUT	DESCRIPTION
1	Optional Ethernet TX connection *(See Ethernet section for details)*
2	Optional Ethernet GND connection *(See Ethernet section for details)*
3	D3, User LED **(BLUE)**
4	D2, Programming status LED **(RED)**
5	D1, Power LED **(GREEN)**
6	Optional ESP8266 ESP-11 Wi-Fi Module header connection
7	Xilinx XADC Analog Input Connection
8	Optional JTAG header *(See Configuration section for details)*
9	D5, User LED, Ethernet Activity LED **(ORANGE)**
10	D4, User LED, Ethernet Link LED **(GREEN)**
11	Optional Ethernet 3.3V connection *(See Ethernet section for details)*
12	Optional Ethernet RX connection *(See Ethernet section for details)*
13	Micro USB port

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POWER SUPPLIES

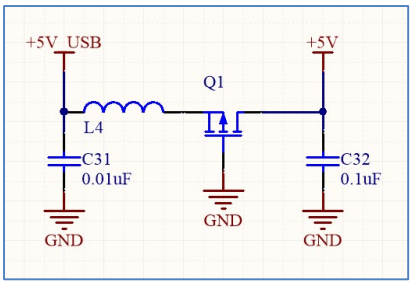

Figure 5: **5V power supply OR switch**

Mercury 2 requires only a single 5V power supply. Power can be supplied either though the +5V power pin (DIP pin 64) or via the Micro-USB connector (+5V_USB). Power can be supplied through both ports at the same time; the P-Channel MOSFET (Q1) ensures that an externally-applied +5V power supply does not flow back into the +5V USB port. **Acceptable external power supply range is 4.5V to 5.5V maximum. Voltages higher than 5.5V on the +5V rail may damage the board.**

The 5V rail directly powers the MCP3008 SPI ADC (U9) and the 3.3V, 1.8V, and 1.0V voltage regulators (U12, U13, U14). The 1.0V regulator powers the FPGA VCCINT and VCCBRAM rails. The 1.8V regulator powers the FPGA VCCAUX rail. The 3.3V regulator powers the remaining components. By default, the FT2232H is configured to enter suspend mode when +5V_USB is absent; this is detected via BCBUS7 (see the FT2232H Datasheet for more details.) 3.3V power is also provided for external devices (DIP pin 63) up to 50mA**. The 3.3V pin is a power output only. Do not connect a power supply to this pin.** The 1.8V and 1.0V regulators are used for internal FPGA power only and are not available externally. Mercury 2 now employs switching regulators to support maximum current requirements across a wide temperature range with minimum heat dissipation.

The current drawn by an FPGA varies greatly depending on the application. During typical use, the Mercury 2 draws an average of 100 – 200 mA, but can draw up to 400mA depending on the application.

CONFIGURATION

At power-on, the Artix-7 FPGA must be configured before it can perform any useful function. The FPGA is essentially a “blank slate” of memory cells and programmable circuit interconnects. A configuration bitstream (*.bit file) must be loaded into the FPGA in order for it to perform a useful function. Xilinx provides a free tool *Vivado WebPACK*, that can be used to create a configuration bitstream from compiled VHDL, Verilog, and/or block diagram source files. *See the MicroNova website for a walkthrough of Vivado WebPack with the Mercury 2 board.*

The Artix-7 FPGA is configured in Master SPI mode via the FPGA mode pins M2, M1, and M0. Upon power-on, the Artix-7 FPGA looks for a valid bitstream in the SPI flash chip (U6). After reading the bitstream and booting successfully, the FPGA_DONE pin goes high, lighting the programming LED (D2). The Artix-7 FPGA can also be programmed directly via the JTAG port, but this configuration is volatile and will be lost if the board is power-cycled. See the *Xilinx 7 Series FPGAs Configuration User Guide (UG470)* for more details on the FPGA configuration and bootup process.

The FTDI FT2232H USB chip (U8) provides a high-speed USB 2.0 interface between the Mercury 2 FPGA development board and a host PC. The FT2232H has two communication channels; channel A is for FPGA configuration and debugging, while channel B is completely free for user applications. *Unlike some other FPGA development board vendors, MicroNova does not keep the details of the FTDI ⇔ FPGA interface hidden from its customers. The complete, unabridged schematics for Mercury 2 are available on the MicroNova website, while the Mercury 2 USB programming application is open-source, released under the permissive MIT License.*

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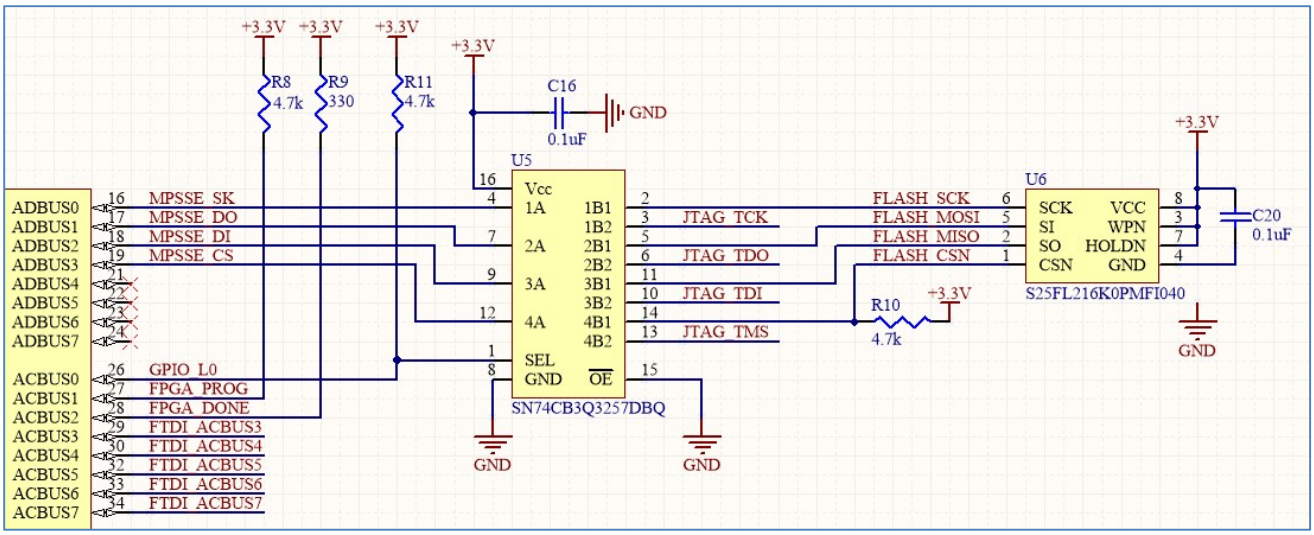

Figure 6: **FTDI-to-FPGA configuration interface**

FTDI channel A is connected directly to the FPGA configuration pins, FPGA_PROG (to initiate an FPGA configuration cycle) and FPGA_DONE (to read back the FPGA configuration status). FTDI channel A is also connected to a digital mux (U5) which is switched between either: the SPI Flash (U6), or the FPGA's JTAG port. The digital mux is controlled via FTDI channel A.

MicroNova provides an open-source programmer utility called **`mercury2_prog`**. The Mercury 2 Programmer utility is a command-line application written in C, and built as a native app for both Linux and Windows. The utility communicates with the FT2232H via FTDI's D2XX driver. The utility writes the specified FPGA bitstream file to the SPI Flash. It is also capable of reading back from the SPI Flash, or erasing the entire SPI Flash. Before accessing the SPI Flash, the FT2232H asserts the FPGA_PROG pin, during which time the FPGA is kept in reset and prevented from reading from the SPI Flash. After accessing the SPI Flash, the FT2232H de-asserts the FPGA_PROG pin, releasing control of the SPI Flash to the FPGA. The FPGA attempts to boot from the SPI Flash, and asserts the FPGA_DONE pin if it has successfully booted.

For most applications, the provided on-board USB port is suitable. For users who require it, the Mercury 2 board also contains an auxiliary JTAG header wired directly to the Artix-7 FPGA (J8). The JTAG port is a 2x3 header with 0.05 inch (1.27mm) spacing. This port may be useful if you would like to connect to the Artix-7 directly using a Xilinx JTAG cable (such as the Platform Cable USB II), or if you want to program the FPGA directly via a microcontroller (see Xilinx XAPP058*: In-System Programming Using an Embedded Microcontroller*).

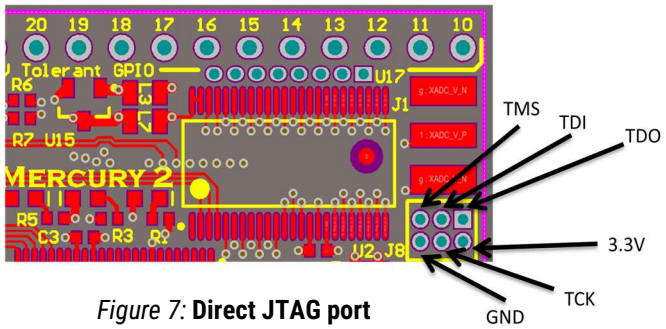

Figure 7: **Direct JTAG port**

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5V TOLERANT DIGITAL I/O

By itself, the Artix-7 FPGA cannot tolerate I/O input voltages greater than V_{CCO} + 0.2V = 3.5V. To provide for greater flexibility, *Mercury 2* is equipped 40 pins of 5V tolerant, general-purpose digital I/O. 5V tolerance is provided by two 20-bit FET bus switches (Texas Instruments SN74CB3T16210) designed specifically for high-speed voltage translation. The CB3T family clamps input signals down to 3.3V so that they do not damage the FPGA input pin.

The 5V tolerant I/O can handle signals up to 100MHz, and have very low propagation delay (0.25ns). The CB3T also provides 2kV ESD protection and undershoot clamp diodes.

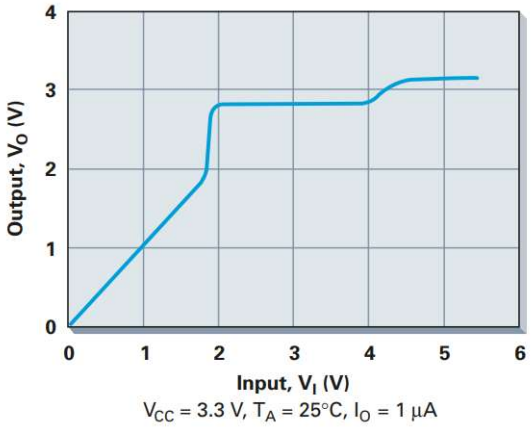

Figure 8: **CB3T Input (DIP pin) vs. Output (FPGA pin)**
(Source: TI Digital Bus Switch Selection Guide)

Please note that the Mercury 2 board does not include series resistors on the 5V tolerant I/O. (This is unlike the Mercury 1 board, which included 150 Ω series resistors on the 5V tolerant I/O. Mercury 2 has dropped series resistors to allow for higher-bandwidth I/O.) The CB3T provides a very small series resistance (5 Ω typical). Take care not to exceed the maximum I/O current ratings for the Artix-7 FPGA. For more details, please see *Xilinx DS181: Artix-7 DC and AC Switching Characteristics*, and *Xilinx UG471: 7 Series FPGAs SelectIO Resources*.

When interfacing with 5V logic, consider whether the device requires 5V CMOS logic levels or 5V TTL logic levels. The level shifting logic onboard *Mercury 2* is made to handle 5V inputs. However, Mercury's I/O pins *output* at 3.3V logic levels. For 5V TTL logic, this is not a problem, as any voltage higher than 2V is interpreted as logic '1'. However, for 5V CMOS logic, the input voltage needs to be 3.5V or higher to be interpreted as a logic '1'. Therefore, when using *Mercury* 2 to drive 5V CMOS inputs, use a pull-up resistor. The pull resistor should be connected between the I/O pin and +5V. Determining the pull-up resistance value is a tradeoff between current draw and I/O speed. Higher resistance values will draw less current, which could be very important when many pull-up resistors are used and/or for battery powered applications. However, higher resistance values will limit the bandwidth of the I/O pin. For most applications, a pull-up resistor between 1kΩ ~ 5kΩ is appropriate.

Please refer to the following table of 5V tolerant digital I/O pins and their corresponding FPGA pins:

5V GPIO	FPGA PIN
0	G1
1	G2
2	F2
3	E1
4	E2
5	C2
6	B2
7	B1
8	A2
9	H2

5V GPIO	FPGA PIN
10	B10
11	C8
12	C9
13	T13
14	R12
15	P11
16	T2
17	T4
18	T5
19	T7

5V GPIO	FPGA PIN
20	K5
21	A3
22	C6
23	D4
24	F5
25	D8
26	P1
27	C7
28	M2
29	N1

5V GPIO	FPGA PIN
30	C1
31	D1
32	L2
33	G5
34	H5
35	H1
36	K1
37	K2
38	J1
39	J3

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EXTERNAL MEMORY

Mercury 2 is equipped with an external 4 Mbit (512k x 8-bit) asynchronous static RAM module.
The SRAM is connected to dedicated pins on the FPGA. Interfacing to the SRAM is performed asynchronously, with read and write cycle times of 10 ns.

To read from the SRAM, perform the following steps:

1. Drive SRAM_CEN low to enable the SRAM, while driving SRAM_WEN high to disable write mode.
2. The contents of the memory location specified by A[18:0] will appear on D[7:0].

To write to the SRAM, perform the following steps:

1. Drive SRAM_CEN low to enable the SRAM, while driving SRAM_WEN low to enable write mode.
2. Data on D[7:0] will be written to memory at the location specified by A[18:0].

The table below specifies the FPGA pins that connect to the SRAM interface. The default configuration of *Mercury 2* uses a 4Mbit SRAM part (ISSI IS61WV5128BLL-10TLI), but 8Mbit and 16Mbit SRAM modules are available as a build-to-order option. Note that the upper address bits A[20:19] are only used on the higher-capacity modules.

5V GPIO	FPGA PIN
A0	M4
A1	N3
A2	N4
A3	P3
A4	M5
A5	E5
A6	D5
A7	D3
A8	B7
A9	B4

5V GPIO	FPGA PIN
A10	J4
A11	H4
A12	H3
A13	G4
A14	E6
A15	A7
A16	A5
A17	A4
A18	C4
A19	J5
A20	C3

5V GPIO	FPGA PIN
D0	L5
D1	L3
D2	L4
D3	R2
D4	F3
D5	F4
D6	E3
D7	D6
WEn	R1
CEn	M6

LEDs

Mercury 2 contains 5 LEDs. D1 (GREEN) illuminates to show the board has power. D2 (RED) illuminates when the FPGA has successfully loaded the configuration bit file. D3 (BLUE) is provided as a user LED and is connected to FPGA pin M1. D4 (GREEN) and D5 (ORANGE) are also user LEDs connected to FPGA pins A14 and A13. *(Optionally, these two LEDs can be wired to ETH_LED1 and ETH_LED2 within the FPGA fabric when using the Ethernet PHY, to monitor Ethernet activity and link state.)*

LED	FPGA PIN	COLOR
D1	*3.3V POWER*	GREEN
D2	*FPGA_DONE*	RED
D3	M1	BLUE
D4	A14	GREEN
D5	A13	ORANGE

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DIRECT I/O

There are ten input/output pins that correct directly to the Artix-7 FPGA without any additional level-shifting circuitry. Three of these inputs are global clock inputs: direct I/O 0 and 1 are single-region clock-capable (SRCC) input pin, while direct I/O 9 is a multi-region clock-capable (MRCC) input pin. Three pairs of the direct I/O can be used as XADC auxiliary inputs. Four pairs can be used as TMDS_33 differential I/O.

DIRECT IO	FPGA PIN	XADC AUX Input	Clock-Capable Input	TMDS pairs
0	C12	n/a	Single-region (SRCC)	Bank 15 L11P
1	C11	n/a	Single-region (SRCC)	Bank 15 L11N
2	D9	n/a	n/a	n/a
3	A9	XADC Aux[8] N	n/a	Bank 15 L2N
4	A8	XADC Aux[8] P	n/a	Bank 15 L2P
5	A10	XADC Aux[1] N	n/a	Bank 15 L3N
6	B9	XADC Aux[1] P	n/a	Bank 15 L3P
7	B6	XADC Aux[12] P	n/a	Bank 35 L2P
8	B5	XADC Aux[12] N	n/a	Bank 35 L2N
9	E12	n/a	Multi-region (MRCC)	n/a

ON-CHIP ANALOG-TO-DIGITAL CONVERTER: XILINX XADC

The Xilinx Artix-7 contains an internal dual-channel 12-bit analog-to-digital converter capable of operating at 1 MSPS. Either channel can be driven by a range of inputs, including the direct coax input, as well as aux inputs on direct I/O pins 3-8. The XADC can also be used to monitor the FPGA internal temperature and power supply rails.

The *Mercury 2* board contains a precision external 1.25V reference (U15) that is connected to the V_{REF} input of the XADC. The XADC can also use an internal reference, this can be accomplished by removing the external reference (U15) and adding a 0Ω resistor to R22. When using the external reference (U15), R22 should not be populated.

The XADC core is controlled and accessed from a user design via the Dynamic Reconfiguration Port (DRP). Refer to the MicroNova website sample code and tutorials dealing with the XADC component. Refer to the Xilinx XADC User Guide (UG480) for more details on XADC usage.

EXTERNAL ANALOG-TO-DIGITAL CONVERTER: MCP3008

Mercury 2 is equipped with an onboard Microchip MCP3008 SPI ADC. It can sample 8-channels with 10-bit resolution, at 200 KSPS sample rate. MCP3008 ADC is capable of sampling voltages in the range of 0V to 5V. This dynamic range is modifiable using the external VREF pin. Communication with the MCP3008 is achieved using SPI. A sample driver in VHDL can be found on the MicroNova website.

ADC PIN	FPGA PIN
ADC SCK	P10
ADC MOSI	J16
ADC MISO	G15
ADC CSN	K15

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EXTERNAL DIGITAL-TO-ANALOG CONVERTER: MCP4812

Mercury 2 is equipped with an onboard Microchip MCP4812 SPI DAC, with two output channels at 10-bit resolution, and an output settling time of 4.5µs (yielding an output data rate of about 220 KSPS). The MCP4812 DAC has a full-scale voltage of 2.048V. *(Note that while the MCP4812 DAC interface includes an option for an output gain of 1 or 2, only the native gain of 1 is usable because the DAC's V_{DD} is powered by 3.3V.)* See the MicroNova website for a sample DAC driver and sine-wave generator project.

DAC PIN	FPGA PIN
DAC SCK	N13
DAC SDI	K12
DAC LDAC	P14
DAC CSN	K16

ETHERNET PHY

Mercury 2 includes a SMSC LAN8720A 10/100 Ethernet PHY. 0.1" header holes are provided on *Mercury 2* for connecting an optional RJ-45 Ethernet jack with integrated magnetics. The SMSC PHY uses the RMII interface and supports 10/100 Mb/s transfer rates. On power-up the PHY is configured with auto-negotiation enabled, advertising all 10/100 modes capable. The PHY chip is configured to use an external clock that must be generated by the FPGA.

OPTIONAL WIRELESS MODULE

Mercury 2 contains an auxiliary 8-pin header (1x8 pin, 0.05") intended for use with the ESP-11 Wi-Fi module, and other pin-compatible wireless modules. Please refer to the Mercury 2 schematic for additional details.

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