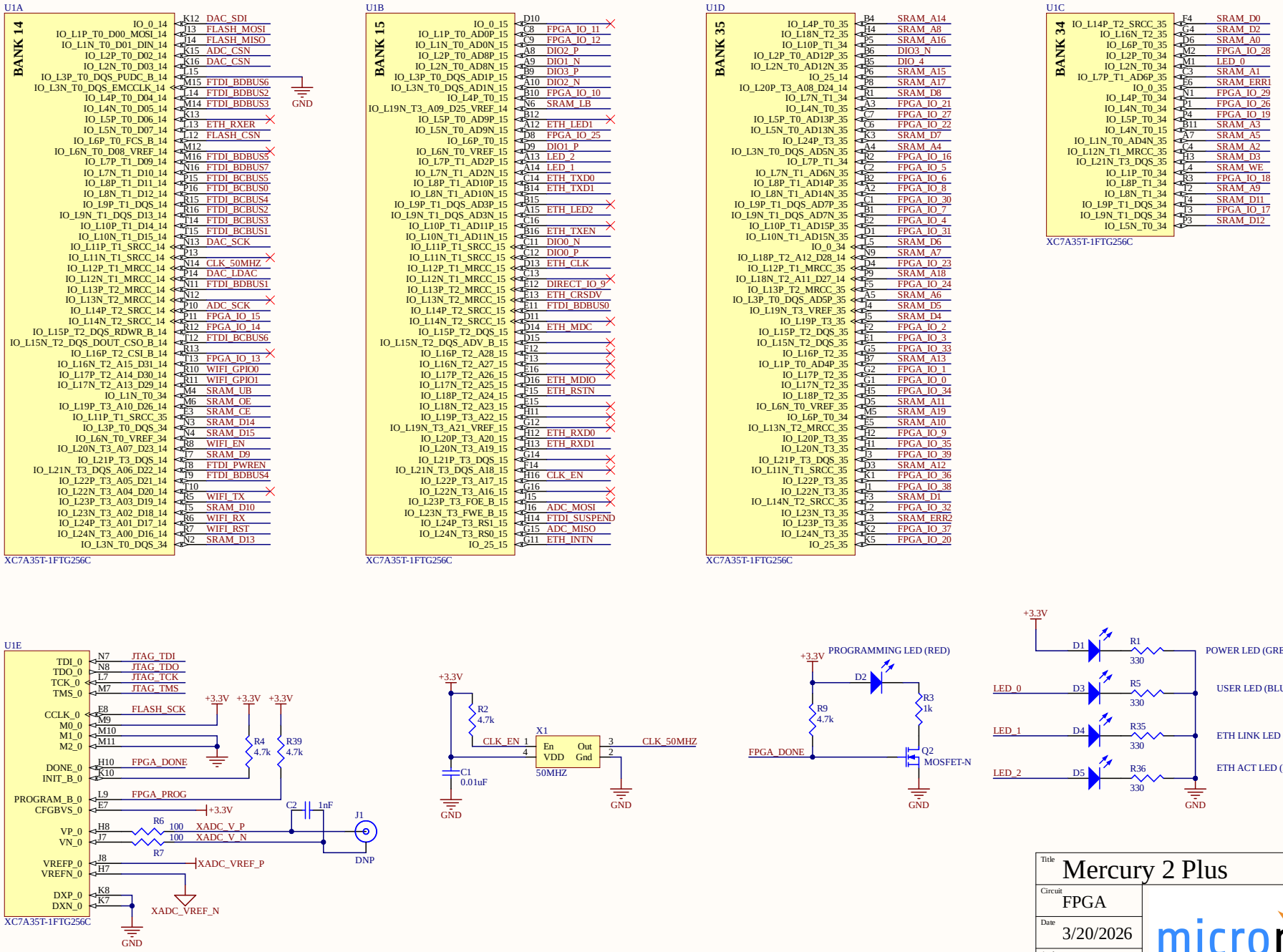
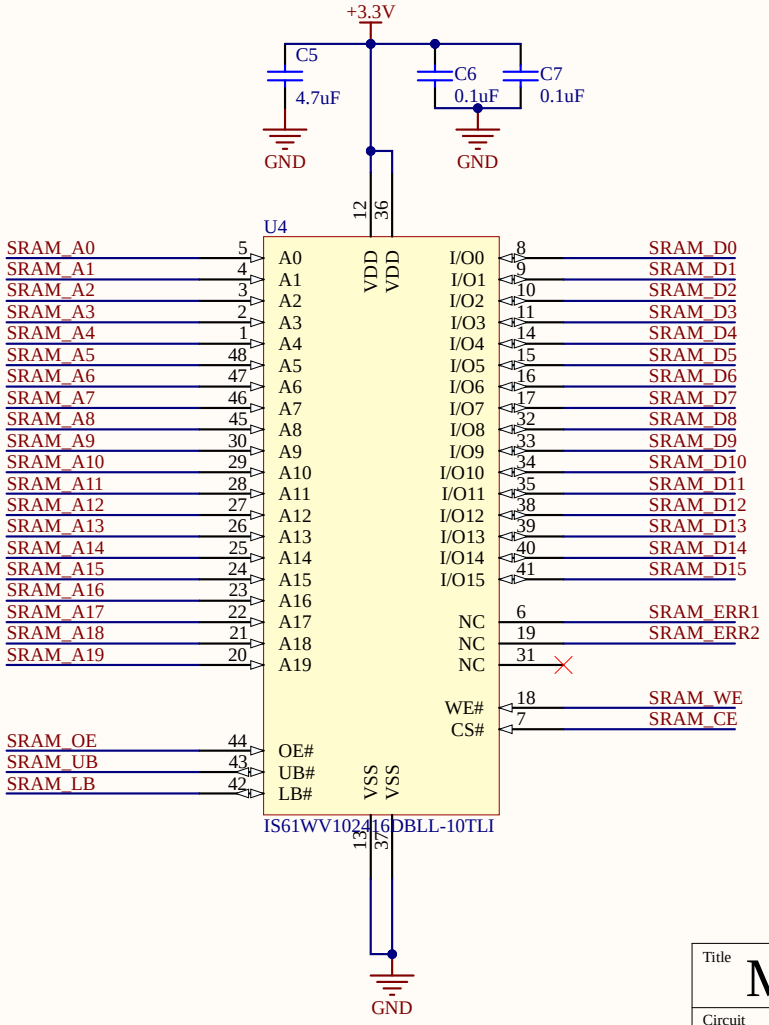


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Rev	1.0
Circuit	FPGA
Date	3/20/2026
Author	RG
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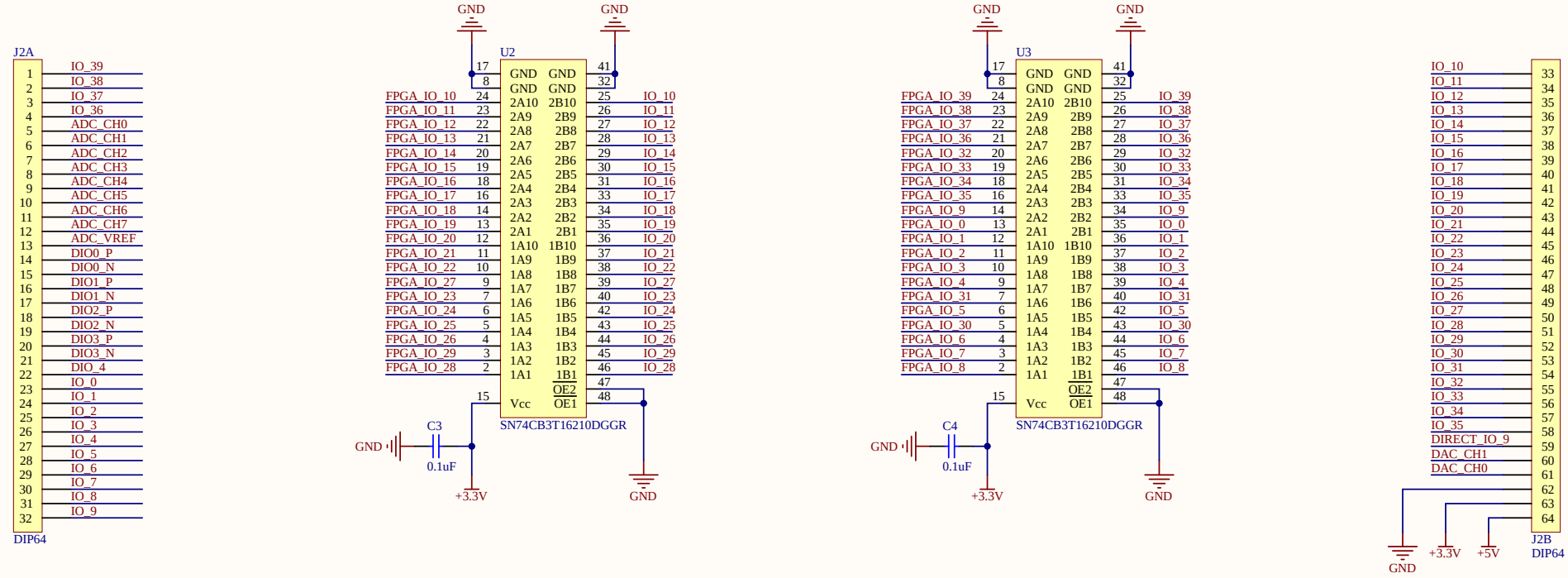
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Title	Mercury 2 Plus	Rev 1.0
Circuit	SRAM	
Date	3/20/2026	
Author	RG	
Sheet #	2 of 7	

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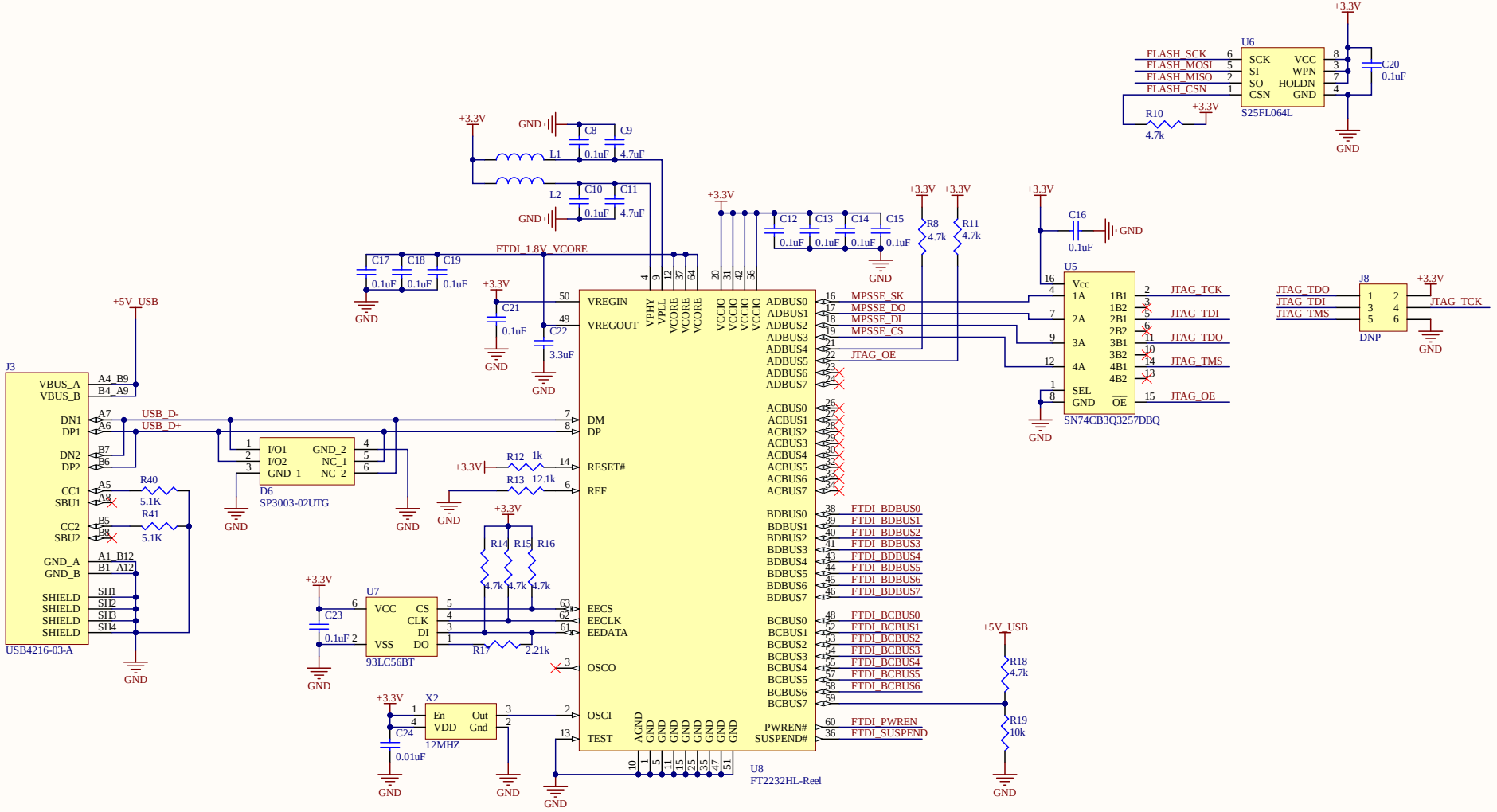
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Circuit	I/O
Date	3/20/2026
Author	RG
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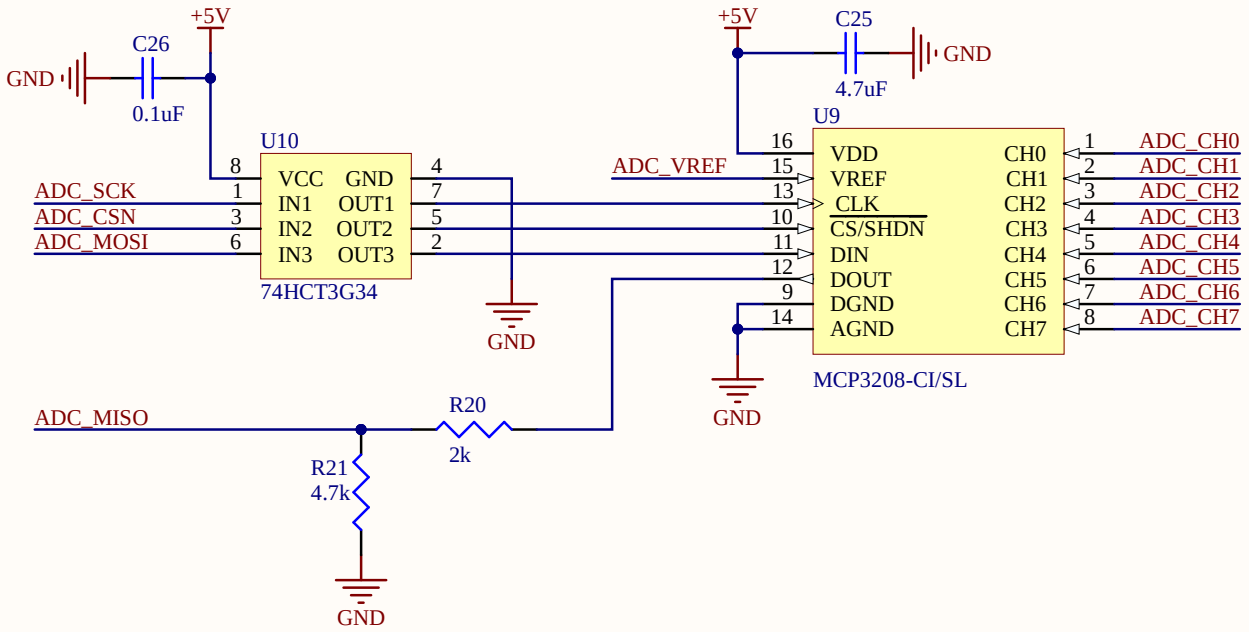


Title	Mercury 2 Plus
Rev	1.0
Circuit	CONFIG
Date	3/20/2026
Author	RG
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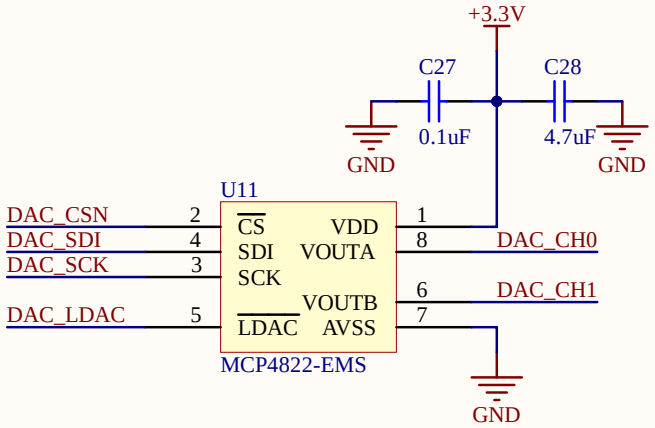
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ADC



DAC

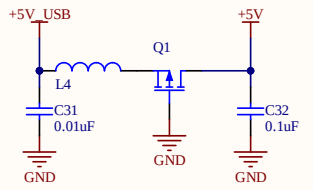


Title	Mercury 2 Plus
Rev	1.0
Circuit	ADC/DAC
Date	3/20/2026
Author	RG
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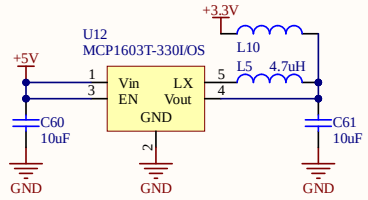
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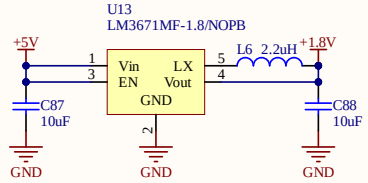
5V POWER INPUT



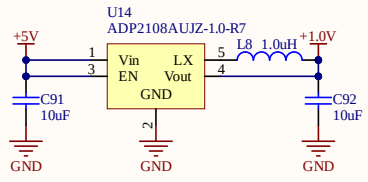
3.3V REGULATOR



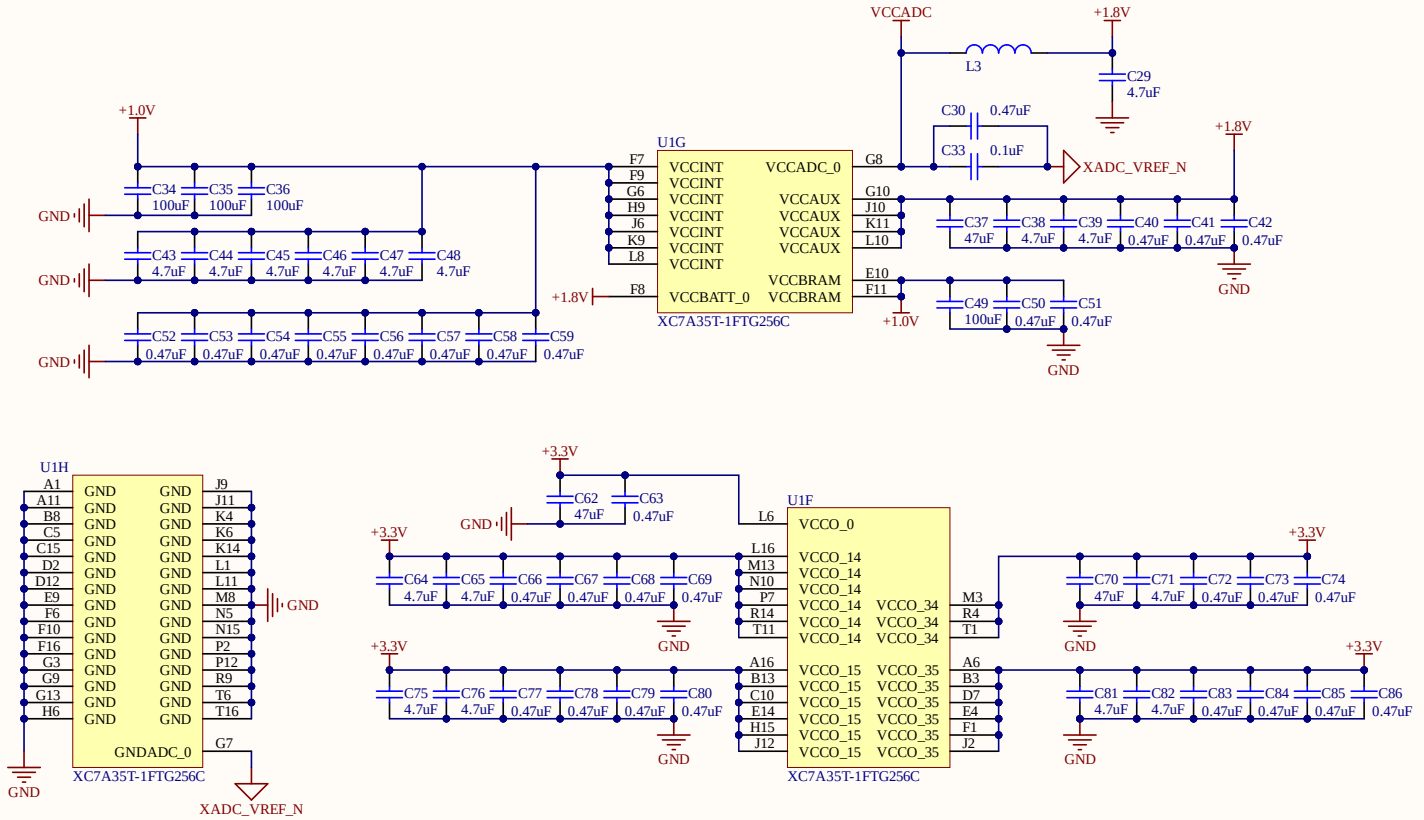
1.8V REGULATOR



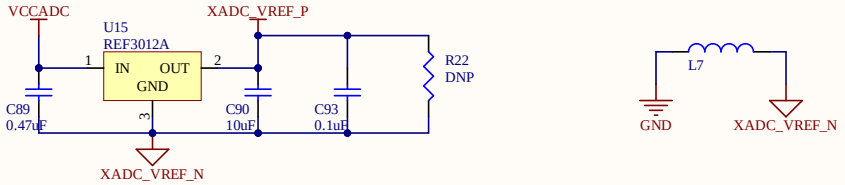
1.0V REGULATOR



FPGA POWER



FPGA XADC REFERENCE

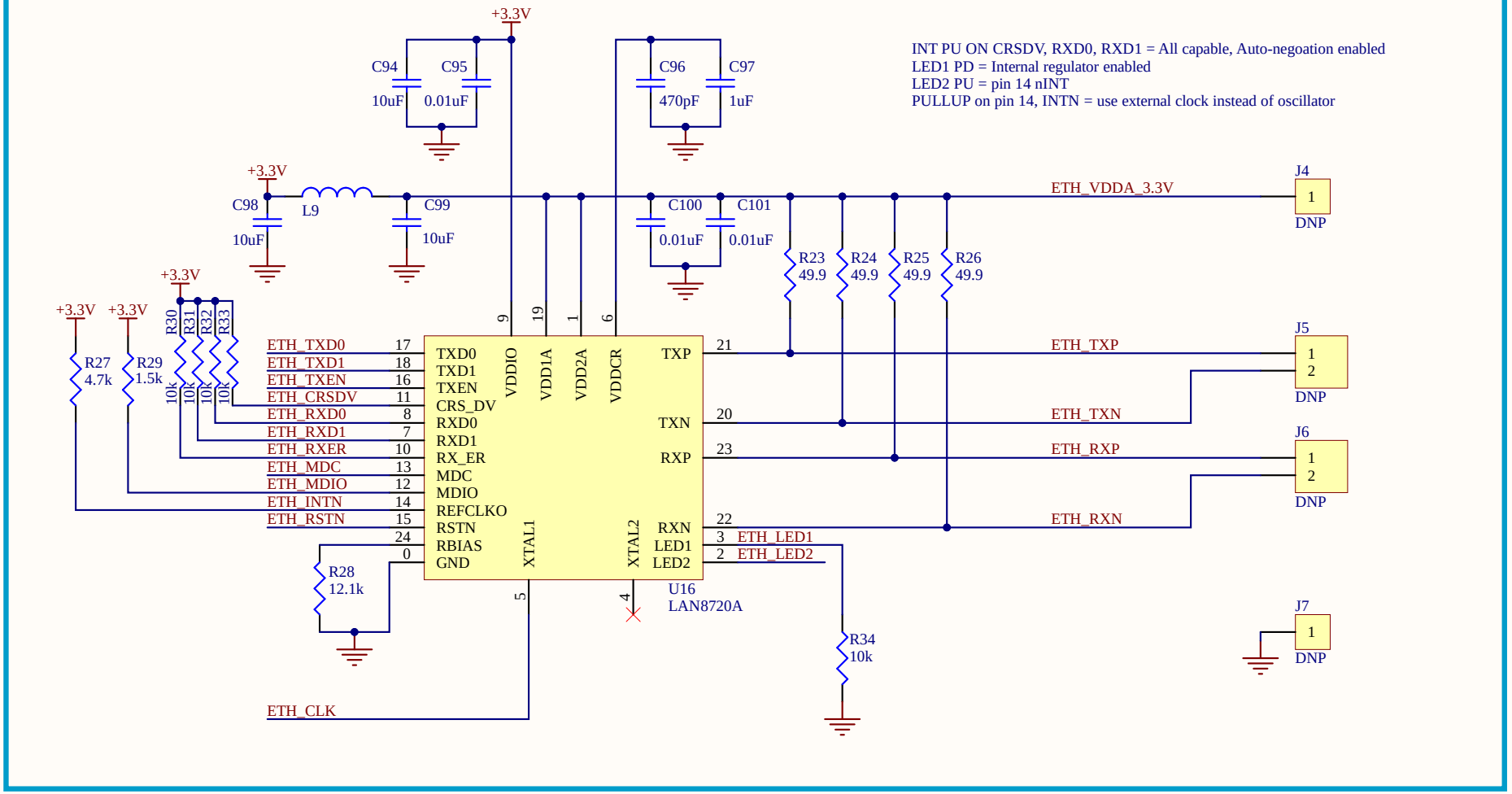


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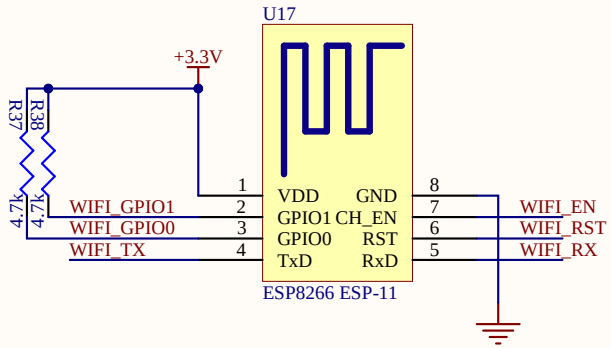
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Optional WiFi



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